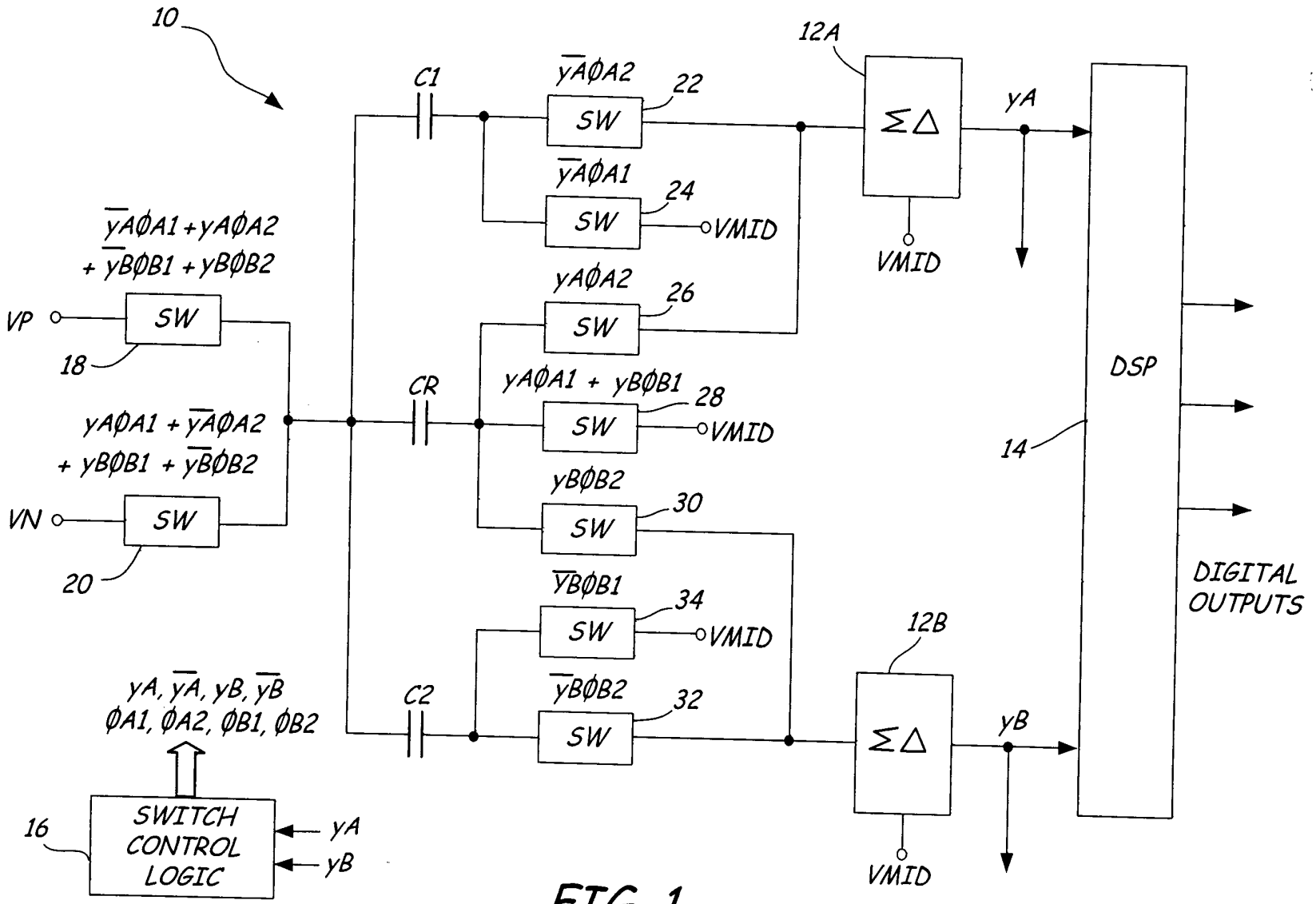
10
C1
$\overline{yA}\emptyset A2$
22
SW
12A
$\Sigma\Delta$
yA
$\overline{yA}\emptyset A1$
24
SW
VMID
VMID
$\overline{yA}\emptyset A1 + yA\emptyset A2$
$+ \overline{yB}\emptyset B1 + yB\emptyset B2$
VP
SW
18
yA∅A2
26
SW
DSP
CR
yA∅A1 + yB∅B1
28
SW
VMID
14
$yA\emptyset A1 + \overline{yA}\emptyset A2$
$+ yB\emptyset B1 + \overline{yB}\emptyset B2$
VN
SW
20
yB∅B2
30
SW
DIGITAL
OUTPUTS
$\overline{yB}\emptyset B1$
34
SW
VMID
12B
yA, $\overline{yA}$, yB, $\overline{yB}$
∅A1, ∅A2, ∅B1, ∅B2
C2
$\overline{yB}\emptyset B2$
32
SW
yB
$\Sigma\Delta$
16
SWITCH
CONTROL
LOGIC
yA
yB
VMID

FIG. 1

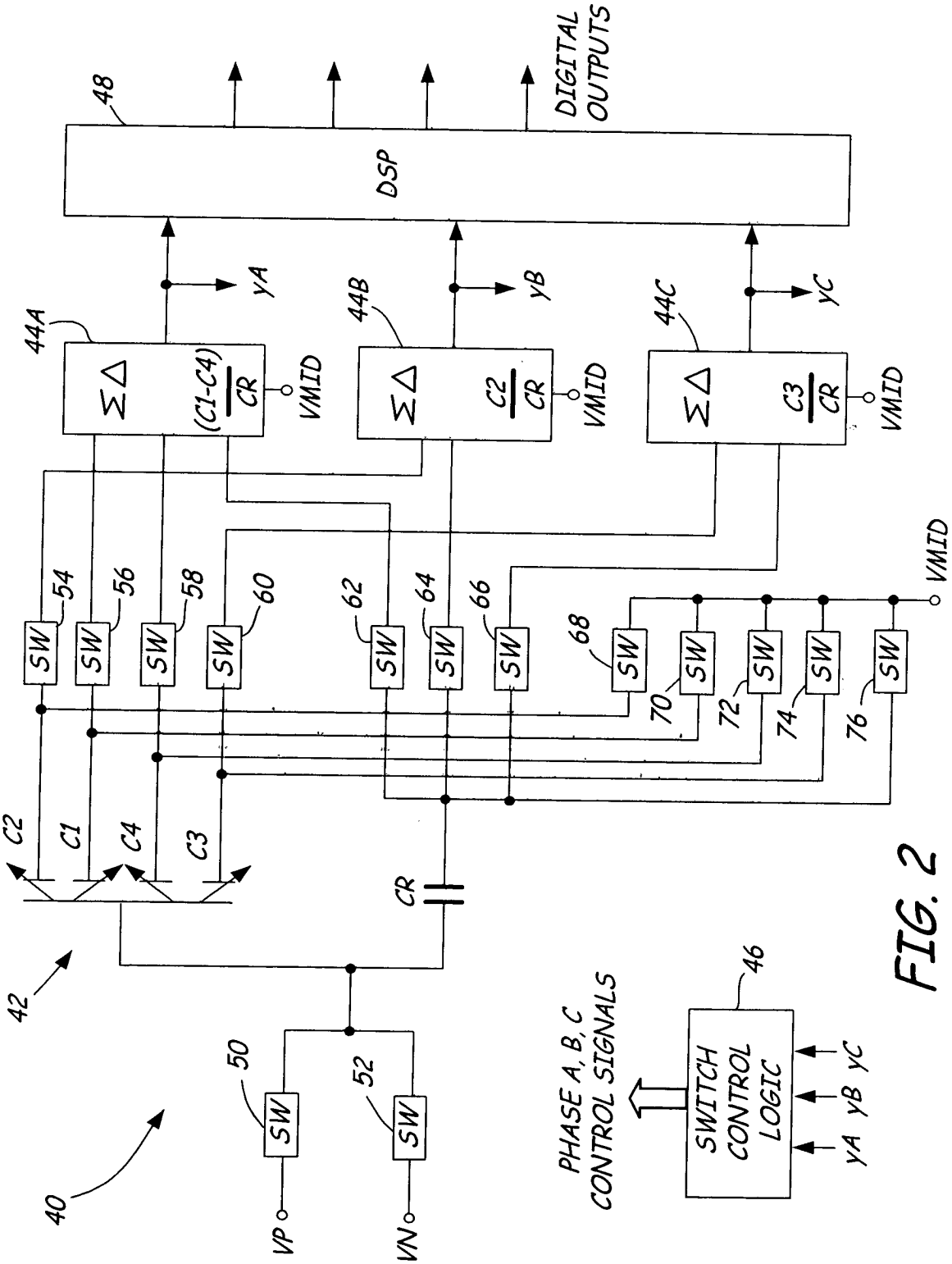
DIGITAL OUTPUTS
48
DSP
44A
44B
44C
ΣΔ
(C1-C4)/CR
C2/CR
C3/CR
VMID
YA
YB
YC
SW
54
56
58
60
62
64
66
68
70
72
74
76
C1
C2
C3
C4
CR
42
40
50
52
VP
VN
PHASE A, B, C CONTROL SIGNALS
SWITCH CONTROL LOGIC
46

FIG. 2